WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a metal contact formed in between adjacent bit lines, said metal contact having an upper portion and a lower portion thereof; and

a metal contact stud for connecting said upper portion to the lower portion, wherein the metal contact stud is formed on a different layer from a layer on which the bit lines are formed.

2. The device of claim 1, wherein the metal contact stud is formed under the bit lines.

3. The device of claim 1, wherein a lower portion of the metal contact stud is smaller in area than an upper portion thereof.

4. The device of claim 1, further comprising:

gate electrodes formed on a substrate having a cell region and a periphery region;

a first insulating layer formed on the substrate and over the gate electrodes, wherein the metal contact studs and the lower portion of the metal contacts are formed through the first insulating layer, said metal contact studs and the metal contacts being comprised of a first conductive material;

a second insulating layer formed on the first insulating layer and

covering the metal contact studs, wherein bit line contacts are formed through the first and second insulating layers, said bit line contacts being comprised of a second conductive material layer; and

a third conductive material layer formed on the second insulating layer and contacting the bit line contacts, wherein the third conductive material layer is patterned to form the bit lines.

5. A method of manufacturing a semiconductor memory device, comprising the steps of:

a) forming gate electrodes on a substrate having a cell region and a periphery region;

b) forming a first insulating layer over the substrate, the first insulating layer covering the gate electrodes;

c) forming first metal contact holes and stud holes in the first insulating layer;

d) forming metal contact studs and first metal contact portions in the stud holes and the first metal contact holes, respectively;

e) forming a second insulating layer on the first insulating layer and on the metal contact studs;

f) forming bit line contact holes passing through the first and second insulating layers;

g) forming bit line contacts in the bit line contact holes; and

h) forming bit lines on the second insulating layer.

6. The method of claim 5, further comprising the steps of:

i) forming a capacitor over the cell region of the substrate;

j) forming a third insulating layer over the substrate, said third insulating layer covering the bit lines;

k) forming second metal contact holes in the second and third insulating layers, the second metal contact holes exposing a portion of the metal contact studs; and

l) forming second metal contacts in the second metal contact holes.

7. The method of claim 5, wherein the step of forming the stud holes further comprises the steps of:

forming a first photoresist pattern on the first insulating layer; and

etching the stud holes in the first insulating layer using the first photoresist pattern as a mask, wherein after the stud holes are formed, the first photoresist pattern is removed.

8. The method of claim 5, wherein the first metal contact holes are formed using anisotropic etching processing to expose a portion of an active area and at least one of said gate electrodes.

9. The method of claim 5, wherein the step of (d) further comprises the steps of:

depositing a first conductive material layer on the first insulating layer, wherein said first conductive material layer fills the stud holes and the first metal contact holes; and

removing a portion of the first conductive material layer to form the metal contact studs and the first metal contact portions.

10. The method of claim 5, wherein the step of (e) further comprises the step of planarizing the second insulating layer using a chemical mechanical polishing (CMP) technique.

11. The method of claim 5, wherein the step of (f) further comprises the steps of:

forming a second photoresist pattern on the second insulating layer; and

etching the first and second insulating layers to form the bit line contact holes using the second photoresist pattern as a mask, wherein after the bit line contact holes are formed, the second photoresist pattern is removed.

12. The method of claim 5, wherein the step of (g) further comprises the steps of:

depositing a second conductive material layer on the second insulating layer, the second conductive material layer filling the bit line contact holes; and

removing a portion of the second conductive material layer on the second insulating layer.

13. The method of claim 5, wherein step (h) further comprises the steps of:

depositing a third conductive material layer on the second insulating layer, wherein the third conductive material layer contact the bit line contacts; and

patterning the third conductive material layer to form the bit lines.

14. The method of claim 5, wherein an area of a lower portion of each metal contact stud is less than an area of an upper portion of each metal contact stud.

15. The method of claim 6, wherein step (k) further comprises the steps of:

forming third photoresist patterns on the third insulating layer;

etching the third insulating layer and the second insulating layer using the third photoresist patterns as a mask to form the second metal contact holes, wherein each of the second metal contact holes pass through between adjacent bit lines and exposes a portion of the metal contact studs.

16. The method of claim 6, wherein step (l) further comprises the steps of:

depositing a fourth conductive material layer on the third insulating layer, the fourth conductive material layer filling the second metal contact holes; and

removing a portion of the fourth conductive material layer on the third insulating layer to form the second metal contacts.

17. The method of claim 12, wherein at least one of the bit line contacts is connected to active area of the substrate.

18. The method of claim 12, wherein at least one of the bit line contacts is connected to one of the gate electrodes.